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Term	Documents
4.USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	62
(L4).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	62

**Database:**

US Patents Full-Text Database  
 US Pre-Grant Publication Full-Text Database  
 JPO Abstracts Database  
 EPO Abstracts Database  
 Derwent World Patents Index  
 IBM Technical Disclosure Bulletins

**Search:**

L5

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**DATE: Monday, July 22, 2002**    [Printable Copy](#)    [Create Case](#)
**Set Name   Query**

side by side

**Hit Count   Set Name**

result set

*DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR*L5    L462    L5*DB=USPT; PLUR=YES; OP=OR*L4    L3 and (substrate or single)62    L4L3    process\$ near4 request\$ near5 (speed or rate) near4 memory87    L3L2    request\$ near5 (speed or rate) near4 memory414    L2L1    request\$ near8 (speed or rate) near4 memory640    L1

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Search Results - Record(s) 1 through 9 of 9 returned.

☐ 1. Document ID: US 6339808 B1

L2: Entry 1 of 9

File: USPT

US-PAT-NO: 6339808

DOCUMENT-IDENTIFIER: US 6339808 B1

TITLE: Address space conversion to retain software compatibility in new architectures

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC
Draw Desc	Image										

☐ 2. Document ID: US 6253304 B1

L2: Entry 2 of 9

File: USPT

US-PAT-NO: 6253304

DOCUMENT-IDENTIFIER: US 6253304 B1

TITLE: Collation of interrupt control devices

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC
Draw Desc	Image										

☐ 3. Document ID: US 6243817 B1

L2: Entry 3 of 9

File: USPT

US-PAT-NO: 6243817

DOCUMENT-IDENTIFIER: US 6243817 B1

TITLE: Device and method for dynamically reducing power consumption within input buffers of a bus interface unit

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC
Draw Desc	Image										

☐ 4. Document ID: US 6199134 B1

L2: Entry 4 of 9

File: USPT

US-PAT-NO: 6199134

DOCUMENT-IDENTIFIER: US 6199134 B1

TITLE: Computer system with bridge logic that asserts a system management interrupt signal when an address is made to a trapped address and which also completes the cycle to the target address

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWC
Draw Desc	Image										

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☐ 5. Document ID: US 6122679 A

L2: Entry 5 of 9

File: USPT

US-PAT-NO: 6122679

DOCUMENT-IDENTIFIER: US 6122679 A

TITLE: Master DMA controller with re-map engine for only spawning programming cycles to slave DMA controllers which do not match current programming cycle

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWC
Draw Desc	Image										

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☐ 6. Document ID: US 6101566 A

L2: Entry 6 of 9

File: USPT

US-PAT-NO: 6101566

DOCUMENT-IDENTIFIER: US 6101566 A

TITLE: Computer system with bridge logic that includes an internal modular expansion bus and a common target interface for internal target devices

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWC
Draw Desc	Image										

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☐ 7. Document ID: US 6070215 A

L2: Entry 7 of 9

File: USPT

US-PAT-NO: 6070215

DOCUMENT-IDENTIFIER: US 6070215 A

TITLE: Computer system with improved transition to low power operation

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWC
Draw Desc	Image									

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☒ 8. Document ID: US 5991833 A

L2: Entry 8 of 9

File: USPT

US-PAT-NO: 5991833

DOCUMENT-IDENTIFIER: US 5991833 A

TITLE: Computer system with bridge logic that reduces interference to CPU cycles during secondary bus transactions

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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KMC

☐ 9. Document ID: US 5969750 A

L2: Entry 9 of 9

File: USPT

US-PAT-NO: 5969750

DOCUMENT-IDENTIFIER: US 5969750 A

TITLE: Moving picture camera with universal serial bus interface

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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Term	Documents
NORTH.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	114528
NORTHS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	10
SOUTH.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	71774
SOUTHS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	10
CPU.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	262252
CPUS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	12433
REQUEST\$3	0
REQUEST.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	232095
REQUESTA.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
REQUESTACK.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
REQUESTB.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	4
((NORTH OR SOUTH) NEAR8 CPU NEAR5 REQUEST\$3).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	9

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L3: Entry 81 of 87

File: USPT

US-PAT-NO: 4152764

DOCUMENT-IDENTIFIER: US 4152764 A

TITLE: Floating-priority storage control for processors in a multi-processor system

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMIC
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☐ 82. Document ID: US 4141067 A

L3: Entry 82 of 87

File: USPT

US-PAT-NO: 4141067

DOCUMENT-IDENTIFIER: US 4141067 A

TITLE: Multiprocessor system with cache memory

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMIC
Draw Desc	Image									

☐ 83. Document ID: US 4126893 A

L3: Entry 83 of 87

File: USPT

US-PAT-NO: 4126893

DOCUMENT-IDENTIFIER: US 4126893 A

TITLE: Interrupt request controller for data processing system

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMIC
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☐ 84. Document ID: US 4080652 A

L3: Entry 84 of 87

File: USPT

US-PAT-NO: 4080652

DOCUMENT-IDENTIFIER: US 4080652 A

TITLE: Data processing system

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMIC

☐ 85. Document ID: US 4080651 A

L3: Entry 85 of 87

File: USPT

US-PAT-NO: 4080651

DOCUMENT-IDENTIFIER: US 4080651 A

TITLE: Memory control processor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMIC

☐ 86. Document ID: US 4037210 A

L3: Entry 86 of 87

File: USPT

US-PAT-NO: 4037210

DOCUMENT-IDENTIFIER: US 4037210 A

TITLE: Computer-peripheral interface

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMIC

☐ 87. Document ID: US 3665415 A

L3: Entry 87 of 87

File: USPT

US-PAT-NO: 3665415

DOCUMENT-IDENTIFIER: US 3665415 A

TITLE: DATA PROCESSING SYSTEM WITH PROGRAM INTERRUPT PRIORITY APPARATUS UTILIZING WORKING STORE FOR MULTIPLEXING INTERRUPT REQUESTS

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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Term	Documents
PROCESS\$3	0
PROCESS.USPT.	1374739
PROCESSA.USPT.	18
PROCESSAB.USPT.	1
PROCESSABI.USPT.	4
PROCESSACH.USPT.	1
PROCESSAED.USPT.	1
PROCESSAL.USPT.	1
PROCESSALL.USPT.	21
PROCESSAND.USPT.	11
PROCESSANI.USPT.	1
(PROCESS\$3 NEAR4 REQUEST\$ NEAR5 (SPEED OR RATE) NEAR4 MEMORY).USPT.	87

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L3: Entry 81 of 87

File: USPT

US-PAT-NO: 4152764

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Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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[KMIC](#)☐ 82. Document ID: US 4141067 A

L3: Entry 82 of 87

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US-PAT-NO: 4141067

DOCUMENT-IDENTIFIER: US 4141067 A

TITLE: Multiprocessor system with cache memory

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

[KMIC](#)☐ 83. Document ID: US 4126893 A

L3: Entry 83 of 87

File: USPT

US-PAT-NO: 4126893

DOCUMENT-IDENTIFIER: US 4126893 A

TITLE: Interrupt request controller for data processing system

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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[KMIC](#)☐ 84. Document ID: US 4080652 A

L3: Entry 84 of 87

File: USPT

US-PAT-NO: 4080652

DOCUMENT-IDENTIFIER: US 4080652 A

TITLE: Data processing system



Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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☐ 85. Document ID: US 4080651 A

L3: Entry 85 of 87

File: USPT

US-PAT-NO: 4080651

DOCUMENT-IDENTIFIER: US 4080651 A

TITLE: Memory control processor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KWC

☐ 86. Document ID: US 4037210 A

L3: Entry 86 of 87

File: USPT

US-PAT-NO: 4037210

DOCUMENT-IDENTIFIER: US 4037210 A

TITLE: Computer-peripheral interface

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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KWC

☐ 87. Document ID: US 3665415 A

L3: Entry 87 of 87

File: USPT

US-PAT-NO: 3665415

DOCUMENT-IDENTIFIER: US 3665415 A

TITLE: DATA PROCESSING SYSTEM WITH PROGRAM INTERRUPT PRIORITY APPARATUS UTILIZING WORKING STORE FOR MULTIPLEXING INTERRUPT REQUESTS

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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PROCESS.USPT.	1374739
PROCESSA.USPT.	18
PROCESSAB.USPT.	1
PROCESSABI.USPT.	4
PROCESSACH.USPT.	1
PROCESSAED.USPT.	1
PROCESSAL.USPT.	1
PROCESSALL.USPT.	21
PROCESSAND.USPT.	11
PROCESSANI.USPT.	1
(PROCESS\$3 NEAR4 REQUEST\$ NEAR5 (SPEED OR RATE) NEAR4 MEMORY).USPT.	87

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